

ABSTRACT OF THE DISCLOSURE

A lateral, high-voltage, FET having a low on-resistance and a buried conduction layer comprises a P-type buried layer region within an N-well formed in a P-type substrate. The P-type buried layer region is connected to a drain electrode by a first P-type drain diffusion region that is disposed in the N-well region. The P-type buried layer region is also connected to a second P-type drain diffusion region that extends down from the surface at one end of the PMOS gate region. A P-type source diffusion region, which connects to the source electrode, defines the other end of the gate region.